App. No. 10/687,128
Office Action Dated February 23, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Claim 4 is amended.

Claims 2, 3, and 12 are canceled.

Listing of Claims:

1. (Previously Presented) A bus control device comprising an external interface connected to an external device via an external system bus, an internal unit, a memory interface connected to an external local memory, and an internal bus at least connecting the external interface to the memory interface and connecting the internal unit to the memory interface,

wherein the memory interface comprises a bus arbiter for arbitrating between a request for use of the internal bus by the external interface and by the internal unit, and a priority processing interval managing part for monitoring a usage pattern of the internal bus based on a result of an arbitration performed by the bus arbiter,

the internal unit has a function of notifying the bus arbiter of an amount of data to be transferred, as well as requesting a use of the internal bus,

the priority processing interval managing part notifies the bus arbiter and the external interface that only the external interface is permitted to use the internal bus, in a case where the internal unit is not using the internal bus and sets a priority processing interval during which only the external interface is capable of using the internal bus,

the bus arbiter compares a previously set amount of data with the amount of data to be transferred, in a case of receiving a request for use of the internal bus and a notification of the amount of data to be transferred from the internal unit, during the priority processing interval,

when the amount of data to be transferred is equal to or less than the previously set amount of data, the bus arbiter permits the internal unit to use the internal bus during the priority processing interval, and

when the amount of data to be transferred exceeds the previously set amount of data, the bus arbiter prohibits the internal unit from using the internal bus while the priority processing interval is set.

2-3. (Canceled)

4. (Currently Amended) [[The]] A bus control device ~~according to claim 2,~~ comprising an external interface connected to an external device via an external system bus, an internal unit, a memory interface connected to an external local memory, and an internal bus at least connecting the external interface to the memory interface and connecting the internal unit to the memory interface,

wherein the memory interface comprises a bus arbiter for arbitrating between a request for use of the internal bus by the external interface and by the internal unit, and a priority processing interval managing part for monitoring [[the]] a usage pattern of the internal bus by confirming a result of an arbitration performed by the bus arbiter at a frequency set by the external device,

the priority processing interval managing part notifies the bus arbiter and the external interface that only the external interface is permitted to use the internal bus, in a case where the internal unit is not using the internal bus and sets a priority processing interval during which only the external interface is capable of using the internal bus,

the bus arbiter prohibits the internal unit from using the internal bus while the priority processing interval is set,

~~wherein~~ the internal unit has a function of notifying the bus arbiter of an amount of data to be transferred, as well as requesting a use of the internal bus,

the bus arbiter compares a previously set amount of data with the amount of data to be transferred, in a case of receiving a request for use of the internal bus and a notification of the amount of data to be transferred from the internal unit, during the priority processing interval, and

when the amount of data to be transferred is equal to or less than the previously set amount of data, the bus arbiter permits the internal unit to use the internal bus during the priority processing interval.

5. (Previously Presented) The bus control device according to claim 1, wherein the priority processing interval managing part monitors the usage pattern of the internal bus by confirming the result of the arbitration performed by the bus arbiter at a previously set frequency, and

the frequency is set by the external device.

6. (Original) A bus control device comprising an external interface connected to an external device via an external system bus, a plurality of internal units, a memory interface connected to an external local memory, and an internal bus connecting the external interface to the memory interface and connecting the internal units to the memory interface,

wherein a part of the plurality of internal units has a function of dividing data to be transferred to the memory interface via the internal bus and transferring it, and

the memory interface prohibits the internal units other than the part of the plurality of internal units from using the internal bus and permits the external interface to use the internal bus, during a period before transfer of all the divided data is completed.

7. (Original) The bus control device according to claim 6, wherein the part of the internal units has a division and transfer notifying part,

the division and transfer notifying part has a function of notifying the memory interface that the divided data is being transferred, during a period before the transfer of all the divided data is completed, in a case of transferring the data after dividing it,

the memory interface has a bus arbiter for arbitrating in a request for use of the internal bus by the external interface and the internal units, and

the bus arbiter prohibits the other internal units from using the internal bus and permits the external interface to use the internal bus, while being notified that the divided data is being transferred.

8. (Original) The bus control device according to claim 6, wherein the part of the internal units comprises a division number setting register for storing information specifying a division number of the data, and divides the data based on the stored information.

9. (Original) The bus control device according to claim 7, wherein the external interface and the other internal units have a function of requesting a use of the internal bus with respect to the bus arbiter and notifying the bus arbiter of an amount of data to be transferred,

the bus arbiter compares a previously set amount of data with the amount of data to be transferred, in a case of receiving a request for use of the internal bus and a notification of the amount of data to be transferred from one or both of the external interface and the other internal units, while being notified that the divided data is being transferred, thereby determining whether or not one or both of the external interface and the other internal units are intended to transfer an amount of data equal to or less than the previously set amount of data, and

the bus arbiter permits the use of the internal bus with respect to those which are determined to be intended to transfer the amount of data equal to or less than the previously set amount of data, while being notified that the divided data is being transferred.

10. (Previously Presented) An information processing system comprising the bus control device of claim 1, a CPU connected to the external interface of the bus control device via a system bus, and a local memory connected to the memory interface of the bus control device.

11. (Previously Presented) An information processing system comprising the bus control device of claim 6, a CPU connected to the external interface of the bus control device via a system bus, and a local memory connected to the memory interface of the bus control device.

12. (Canceled)

13. (Previously Presented) The bus control device according to claim 1, wherein the memory interface comprises a priority processing interval setting register for storing information specifying a length of the priority processing interval, and

the priority processing interval managing part sets the priority processing interval based on the information stored in the priority processing interval setting register.